

What is claimed is:

1. A method for detecting whether an IDE drive is connected to an intelligent drive electronics channel within a computer, comprising:

reading a status register destination for the IDE drive; and

based on a value read from the status register destination, determining whether the IDE drive is connected.

2. The method of claim 1, wherein determining whether the IDE drive is connected comprises:

detecting whether data read from the status register destination has a first predefined value; and

upon the data read from the status register destination not having the first predefined value, returning that the IDE drive is connected to the intelligent drive electronics channel.

3. The method of claim 1, prior to reading the status register destination, further comprising:

writing data to a drive head register destination for the IDE drive;

reading the drive head register destination;

detecting whether the data read from the drive head register destination matches the data written to the drive head register destination;

in response to the data read from the drive head register destination not matching the data written to the drive head register destination, returning that the IDE drive is not connected to an intelligent drive electronics channel; and

in response to the data read from the drive head register destination matching the data written to the drive head register destination, reading the status register destination.

4. The method of claim 3, further comprising:
 - prior to writing data to a drive head register destination for the IDE drive, establishing a drive selection value for each IDE drive; and
 - selecting the IDE drive for detection by writing a drive selection value to the drive head register destination.
5. The method of claim 2, further comprising:
 - upon the data read from the status register destination having the first predefined value, reading a cylinder low register destination and a cylinder high register destination of the drive;
 - detecting whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature;
 - in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, returning that the IDE drive is connected to the intelligent drive electronics channel.
6. The method of claim 5, wherein the IDE drive connected to the intelligent drive electronics channel implements a packet command feature set.
7. The method of claim 5, further comprising in response to the data read from cylinder low register destination and the cylinder high register destination not matching the predefined signature, returning that the IDE drive is not connected to an intelligent drive electronics channel.
8. The method of claim 7, wherein the predefined signature comprises a second predefined value of the cylinder high register destination and a third predefined value of the cylinder low register destination.
9. The method of claim 4, wherein two IDE drives may be connected per intelligent drive electronics channel and wherein a one of the IDE drives comprises a master drive and a one of the IDE drives comprises a slave drive.

10. The method of claim 9, wherein the drive selection value represents at least one of the master drive and the slave drive.

11. The method of claim 4 further comprising, prior to reading a status register destination, resetting the computer.

12. The method of claim 11, wherein resetting the computer comprises executing at least one of the following:

- a power on reset of the computer;
- a hardware reset;
- an execute drive diagnostics command;
- a software reset; and
- a drive reset.

13. The method of claim 1, wherein the IDE drive comprises at least one of the following:

- a hard disk drive;
- a floppy drive;
- a CD ROM disk drive; and
- a tape drive.

14. A computer program product comprising a computer readable medium having control logic stored therein for causing a computer to detect whether an IDE drive is connected to an intelligent drive electronics channel within the computer, said control logic comprising computer readable program code means for causing the computer to:

read a status register destination for the IDE drive;

detect whether data read from the status register destination has a first predefined value; and

upon the data read from the status register destination not having the first predefined value, return a first indication that an IDE drive is connected to the intelligent drive electronics channel.

15. The computer program product of claim 14, prior to causing the computer to read the status register destination, further comprising computer readable code means for causing the computer to:

establish a drive selection value for each IDE drive wherein each IDE drive comprises at least one of a master IDE device and a slave IDE device;

select the IDE drive for detection by writing data to a drive head register destination for the IDE drive wherein the data includes the drive selection value established for the IDE drive;

read the drive head register destination;

detect whether the data read from the drive head register destination matches the data written to the drive head register destination;

in response to the data read from the drive head register destination not matching the data written to the drive head register destination, return a second indication that the IDE drive is not connected to the intelligent drive electronics channel; and

in response to the data read from the drive head register destination matching the data written to the drive head register destination, read the status register destination.

16. The computer program product of claim 14, further comprising computer readable code means for causing the computer to:

upon the data read from the status register destination having the first predefined value, read a cylinder low register destination and a cylinder high register destination for the IDE drive;

detect whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature;

in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, return the first indication that the IDE drive is connected to the intelligent drive electronics channel.

17. The computer program product of claim 16, wherein the IDE drive connected to the intelligent drive electronics channel implements a packet command feature set.

18. The method of claim 16, wherein the predefined signature comprises a second predefined value of the cylinder high register destination and a third predefined value of the cylinder low register destination.

19. A computer system for detecting whether an IDE drive is connected to an intelligent drive electronics channel within the computer system, the computer system comprising:

- a processor coupled to a memory;

- at least one bus coupled to the processor and capable of hosting at least one IDE drive via an intelligent drive electronics channel; and

- a basic input/output system program capable of being executed on the processor and, when executed on the processor, operative to:

 - read a status register destination for the IDE drive;

 - detect whether data read from the status register destination has a first predefined value; and

 - upon the data read from the status register destination not having the first predefined value, return a first indication that an IDE drive is connected to the intelligent drive electronics channel.

20. The computer system of claim 19, wherein prior to reading the status register destination, the basic input/output system program is further operative to:

- establish a drive selection value for each IDE drive wherein each IDE drive comprises at least one of a master IDE device and a slave IDE device;

- select the IDE drive for detection by writing data to a drive head register destination for the IDE drive wherein the data includes the drive selection value established for the IDE drive;

 - read the drive head register destination;

 - detect whether the data read from the drive head register destination matches the data written to the drive head register destination;

 - in response to the data read from the drive head register destination not matching the data written to the drive head register destination, return a second indication that the IDE drive is not connected to the intelligent drive electronics channel; and

 - in response to the data read from the drive head register destination matching the data written to the drive head register destination, read the status register destination.

21. The computer system of claim 19, the basic input/output system program is further operative to:

upon the data read from the status register destination having the first predefined value, read a cylinder low register destination and a cylinder high register destination for the IDE drive;

detect whether data read from the cylinder low register destination and the cylinder high register destination matches a predefined signature;

in response to the data read from cylinder low register destination and the cylinder high register destination matching the predefined signature, return the first indication that the IDE drive is connected to the intelligent drive electronics channel

22. A method for detecting whether an ATAPI device is connected to an intelligent drive electronics channel within a computer, comprising:

reading a cylinder high register destination and a cylinder low register destination for the ATAPI device; and

based on a first value read from the cylinder high register destination and a second value read from the cylinder low register destination, determining whether the ATAPI device is connected.

23. The method of claim 22, wherein determining whether the ATAPI device is connected comprises:

detecting whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, returning that the ATAPI device is connected to the intelligent drive electronics channel.

24. The method of claim 23, prior to reading at least one of the cylinder high register destination and the cylinder low register destination, further comprising:

reading a status register destination for the ATAPI device; and

detecting that the data read from the status register destination has a third predefined value.

25. The method of claim 23, prior to reading the status register destination further comprising:

- establishing a device selection value for one or more ATAPI devices wherein each ATAPI device comprises at least one of a master IDE device and a slave IDE device;

- selecting the ATAPI device for detection by writing data to a device head register destination for the ATAPI device wherein the data includes the device selection value established for the ATAPI device;

- reading the device head register destination after writing the data;

- detecting whether the data read from the device head register destination matches the data written to the device head register destination; and
in response to the data read from the device head register destination matching the data written to the device head register destination, reading the status register destination.

26. The method of claim 22, wherein the ATAPI device comprises at least one of the following:

- a hard disk drive;

- a floppy drive;

- a CD ROM disk drive; and

- a tape drive.

27. A computer program product comprising a computer readable medium having control logic stored therein for causing a computer to detect whether an ATAPI drive is connected to an intelligent drive electronics channel within the computer, said control logic comprising computer readable program code means for causing the computer to:

- read a cylinder high register destination and a cylinder low register destination for the ATAPI drive;

- detect whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

- upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, return an indication that the ATAPI drive is connected to the intelligent drive electronics channel.

28. The computer program product of claim 27, prior to causing the computer to read at least one of the cylinder high register destination and the cylinder low register destination, further comprising computer readable program code means for causing the computer to:

- read a status register destination for the ATAPI drive; and

- detect that the data read from the status register destination has a third predefined value.

29. A computer system operative to detect whether an ATAPI drive is connected to an intelligent drive electronics channel within the computer, said computer system comprising:

- a processor coupled to a memory;

- at least one bus coupled to the processor and capable of hosting at least one ATAPI drive via an intelligent drive electronics channel; and

- a basic input/output system program capable of being executed on the processor and, when executed on the processor, operative to:

 - read a cylinder high register destination and a cylinder low register destination for the ATAPI drive;

 - detect whether data read from the cylinder high register destination has a first predefined value and whether data read from the cylinder low register destination has a second predefined value; and

 - upon the data read from the cylinder high register destination having the first predefined value and the data read from the cylinder low register destination having the second predefined value, return an indication that the ATAPI drive is connected to the intelligent drive electronics channel.

30. The computer system of claim 29, wherein prior to reading at least one of the cylinder high register destination and the cylinder low register destination, the basic input/output system program is further operative to:

- read a status register destination for the ATAPI drive; and

- detect that the data read from the status register destination has a third predefined value.